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EXAMINER

GANDHI, DIPAKKUMAR B

ART UNIT PAPER NUMBER

2138

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/681,244

Applicant(s)

BAUMER ET AL.

Examiner

Dipakkumar Gandhi

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-53 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-53 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1, 13-18, 23, 24, 35-38, 41, 42, 44, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) in view of Butler et al. (US 6,438,717 B1).

As per claim 1, Pierson teaches an integrated packet bit error rate tester comprising: an interface for programming the packet transmit and packet receive circuits, wherein the packet transmit circuit can generate an arbitrary packet pattern in response to commands from the interface, and wherein the packet receive circuit can determine a bit error rate of the channel under test (fig. 4, fig. 7, page 6, paragraph 73, page 10-11, paragraph 128, page 11, paragraph 129, 131, 132, page 12, paragraph 143, 144, Pierson). However Pierson does not explicitly teach the specific use of a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test; a packet receive circuit including a second memory for storing received packet compare data and connectable to the channel under test.

Butler et al. in an analogous art teach that the interface control block 3...highest bit error rates inactive (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.). Butler et al. also teach that FIG. 3 illustrates...respective register per channel are read (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

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Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Butler et al. by including an additional step of using a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test; a packet receive circuit including a second memory for storing received packet compare data and connectable to the channel under test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit the stored data and verify the stored received data during slow periods in data packet transmission and processing or when the card is running through self testing and diagnostics.

- As per claim 13, Pierson and Butler et al. teach the additional limitations.

Pierson teaches that the arbitrary packet pattern is received from an external RAM (page 11, paragraph 129, Pierson).

- As per claim 14, Pierson and Butler et al. teach the additional limitations.

Pierson teaches that the arbitrary packet pattern can be loaded into a Random Access Memory for bit error rate testing (page 11, paragraph 129, Pierson).

- As per claim 15, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data only after a pre-programmed pattern is lost (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 16, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data only after an error is detected (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 17, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data immediately (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 18, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that a finite state machine for controlling the capture of the received data (comparison and control 34 in fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

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- As per claim 23, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the arbitrary packet pattern is a 10G SERDES packet (col. 2, lines 53-60, Butler et al.).

- As per claim 24, Pierson and Butler et al. teach the additional limitations.

Pierson teaches an integrated packet bit error rate tester comprising: an interface for programming the packet transmit and packet receive circuits, and wherein the packet receive circuit can determine a bit error rate of the channel under test based on the transmit packet data compared to the receive packet data (fig. 4, fig. 7, page 6, paragraph 73, page 10-11, paragraph 128, page 11, paragraph 129, 131, 132, page 12, paragraph 143, 144, Pierson).

Butler et al. teach a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test; a packet receive circuit including a second memory for capturing received packet compare data from the channel under test; wherein the packet transmit circuit can generate an arbitrary SERDES packet pattern in response to commands from the interface (fig. 1, 3, col. 2, line 53 to col. 3, line 16, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 35, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data only after a pre-programmed pattern is lost (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 36, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data only after an error is detected (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 37, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach that the second memory captures the received packet data immediately (fig. 3, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 38, Pierson and Butler et al. teach the additional limitations.

Pierson teaches an integrated packet bit error rate tester (fig. 4, fig. 7, page 10-11, paragraph 128, Pierson).

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Butler et al. teach a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test; and a packet receive circuit including a second memory for capturing received packet data from the channel under test upon any one of (a) after a pre-programmed pattern is detected, (b) after a pre-programmed pattern is lost, (c) after an error is detected, and (d) immediately (fig. 1, col. 2, line 53 to col. 3, line 16, col. 3, line 39 to col. 4, line 13, Butler et al.)

- As per claim 41, Pierson and Butler et al. teach the additional limitations.

Pierson teaches a method of testing bit error rate of a channel comprising: generating a test packet including an arbitrary marker pattern; and determining the bit error rate of the channel based on the test packet (fig. 4, fig. 7, page 6, paragraph 73, page 10-11, paragraph 128, page 11, paragraph 129, 131, 132, page 12, paragraph 143, 144, Pierson).

Butler et al. teach transmitting the test packet over the channel; capturing the test packet from the channel (fig. 1, col. 2, line 53 to col. 3, line 16, col. 3, line 39 to col. 4, line 13, Butler et al.).

- As per claim 42, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach an arbitrary 10G SERDES packet pattern (col. 2, lines 53-65, Butler et al.).

Pierson teaches generating packet pattern (pages 10-11, paragraph 128, Pierson).

- As per claim 44, Pierson and Butler et al. teach the additional limitations.

Butler et al. teach an arbitrary 10G SERDES packet pattern (col. 2, lines 53-65, Butler et al.).

Pierson teaches programming the arbitrary packet pattern through a media independent input/output interface (pages 10-11, paragraph 128, Pierson).

- As per claim 51, Pierson and Butler et al. teach the additional limitations.

Pierson teaches determining a bit error rate of the channel under test (page 11, paragraph 129, Pierson).

4. Claims 2-3, 29-30, 39-40, 43, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) and Butler et al. (US 6,438,717 B1) as applied to claim 1 above, and further in view of Hillman et al. (US 6,140,956).

As per claim 2, Pierson and Butler et al. substantially teach the claimed invention described in claim 1 (as rejected above).

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However Pierson and Butler et al. do not explicitly teach specifically that the packet transmit circuit includes a first pseudo-random number generator for generating the arbitrary packet pattern.

Hillman et al. in an analogous art teach that the data in the data packet is randomized before transmission by using a pseudo-random code sequence. The pseudo random code is generated by a pseudo-random number generator from a seed value (col. 15, lines 29-32, Hillman et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Hillman et al. by including an additional step of using the packet transmit circuit that includes a first pseudo-random number generator for generating the arbitrary packet pattern.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to transmit random data pattern for testing.

- As per claim 3, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Hillman et al. teach that the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary packet pattern that is generated by the first pseudo-random number generator (col. 15, lines 35-41, Hillman et al.).

- As per claim 29, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Hillman et al. teach that the packet transmit circuit includes a first pseudo-random number generator (col. 15, lines 29-32, Hillman et al.).

Butler et al. teach generating the arbitrary SERDES packet pattern (col. 2, lines 53-60, Butler et al.).

- As per claim 30, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Hillman et al. teach that the packet receive circuit includes a second pseudo-random number generator for generating the same packet pattern that is generated by the first pseudo-random number generator (col. 15, lines 35-41, Hillman et al.).

Butler et al. teach generating the arbitrary SERDES packet pattern (col. 2, lines 53-60, Butler et al.).

- As per claim 39, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

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Hillman et al. teach that the packet transmit circuit includes a first pseudo-random number generator (col. 15, lines 29-32, Hillman et al.).

Butler et al. teach the arbitrary SERDES packet pattern for transmission over the channel under test (col. 2, lines 53-60, Butler et al.).

Pierson teaches generating packet pattern (pages 10-11, paragraph 128, Pierson).

- As per claim 40, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Hillman et al. teach that the packet receive circuit includes a second pseudo-random number generator for generating the same packet pattern that is generated by the first pseudo-random number generator (col. 15, lines 35-41, Hillman et al.).

Butler et al. teach generating the arbitrary SERDES packet pattern (col. 2, lines 53-60, Butler et al.).

- As per claim 43, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Butler et al. teach an arbitrary 10G SERDES packet pattern (col. 2, lines 53-65, Butler et al.).

Pierson teaches generating packet pattern (pages 10-11, paragraph 128, Pierson).

Hillman et al. teach that a first pseudo-random number generator (col. 15, lines 29-32, Hillman et al.).

- As per claim 45, Pierson, Butler et al. and Hillman et al. teach the additional limitations.

Butler et al. teach an arbitrary 10G SERDES packet pattern (col. 2, lines 53-65, Butler et al.).

Pierson teaches generating packet pattern (pages 10-11, paragraph 128, Pierson).

Hillman et al. teach generating the same arbitrary packet pattern using a second pseudo-random number generator as the packet pattern generated by the first pseudo-random number generator (col. 15, lines 35-41, Hillman et al.).

5. Claims 4-5, 19-22, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) and Butler et al. (US 6,438,717 B1) as applied to claim 1 above, and further in view of Morikawa (US 2002/0054569 A1).

As per claim 4, Pierson and Butler et al. substantially teach the claimed invention described in claim 1 (as rejected above). Pierson also teaches packet transmit circuit and bit error rate testing (page 11, paragraph 129, Pierson).



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However Pierson and Butler et al. do not explicitly teach specific use of a byte counter for counting the number of bytes transmitted.

Morikawa in an analogous art teaches transmitted byte counter (fig. 1B, page 6, paragraph 92, Morikawa).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Morikawa by including an additional step of using a byte counter for counting the number of bytes transmitted.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a byte counter for counting the number of bytes transmitted would provide the opportunity to compare the number of bytes transmitted with the number of bytes received and determine transmission error for number of bytes lost.

- As per claim 5, Pierson, Butler et al. and Morikawa teach the additional limitations.

Pierson teaches packet transmit circuit and bit error rate testing (page 11, paragraph 129, Pierson).

Morikawa teach a packet counter for counting the number of packets transmitted (page 3, paragraph 46, Morikawa).

- As per claim 19, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a byte counter for counting a total number of bytes received (page 6, paragraph 92, Morikawa).

- As per claim 20, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a packet counter for counting a total number of packets received (page 4, paragraph 61, Morikawa).

- As per claim 21, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet transmit circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a byte counter for counting a total number of bytes transmitted (page 6, paragraph 92, Morikawa).

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- As per claim 22, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet transmit circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a packet counter for counting a total number of packets transmitted (page 3, paragraph 46, Morikawa).

- As per claim 25, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a byte counter for counting a total number of bytes received (page 6, paragraph 92, Morikawa).

- As per claim 26, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a packet counter for counting a total number of packets received (page 4, paragraph 61, Morikawa).

- As per claim 27, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet transmit circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a byte counter for counting a total number of bytes transmitted (page 6, paragraph 92, Morikawa).

- As per claim 28, Pierson, Butler et al. and Morikawa teach the additional limitations.

Butler et al. teach the packet transmit circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Morikawa teach a packet counter for counting a total number of packets transmitted (page 3, paragraph 46, Morikawa).

- As per claim 46, Pierson, Butler et al. and Morikawa teach the additional limitations.

Morikawa teach counting a number of bytes received (page 6, paragraph 92, Morikawa).

Pierson teaches the bit error rate testing (page 11, paragraph 129, Pierson).

- As per claim 47, Pierson, Butler et al. and Morikawa teach the additional limitations.

Morikawa teach a number of packets received (page 4, paragraph 61, Morikawa).

Pierson teaches the bit error rate testing (page 11, paragraph 129, Pierson).

- As per claim 52, Pierson, Butler et al. and Morikawa teach the additional limitations.

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Morikawa teach counting a number of packets transmitted over the channel (page 3, paragraph 46, Morikawa).

- As per claim 53, Pierson, Butler et al. and Morikawa teach the additional limitations.

Morikawa teach counting a number of bytes transmitted over the channel (fig. 1B, page 6, paragraph 92, Morikawa).

6. Claims 6-7, 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) and Butler et al. (US 6,438,717 B1) as applied to claim 1 above, and further in view of Chen et al. (US 5,726,991).

As per claim 6, Pierson and Butler et al. substantially teach the claimed invention described in claim 1 (as rejected above). Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

However Pierson and Butler et al. do not explicitly teach specific use of a bit error counter for counting a number of bit errors detected during bit error rate testing.

Chen et al. in an analogous art teach that a counter means is coupled to the receiver for counting each generated bit error for establishing the bit error rate (col. 2, lines 11-13, Chen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Chen et al. by including an additional step of using a bit error counter for counting a number of bit errors detected during bit error rate testing.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a bit error counter for counting a number of bit errors detected during bit error rate testing would provide the opportunity to detect data transmission errors.

- As per claim 7, Pierson, Butler et al. and Chen et al. teach the additional limitations.

Butler et al. teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

Chen et al. teach a byte error counter for counting a number of bytes with at least one bit in error detected during bit error rate testing (col. 5, lines 13-15, Chen et al.).

- As per claim 48, Pierson, Butler et al. and Chen et al. teach the additional limitations.

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Chen et al. teach counting a number of bit errors detected during the bit error rate testing (col. 2, lines 11-13, Chen et al.).

- As per claim 49, Pierson, Butler et al. and Chen et al. teach the additional limitations.

Chen et al. teach counting a number of bytes with errors detected during the bit error rate testing (col. 5, lines 13-15, Chen et al.).

7. Claims 8, 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) and Butler et al. (US 6,438,717 B1) as applied to claim 1 above, and further in view of Yu (US 2001/0012288 A1).

As per claim 8, Pierson and Butler et al. substantially teach the claimed invention described in claim 1 (as rejected above). Butler et al. also teach the packet receive circuit (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.). Pierson also teaches the bit error rate testing (page 11, paragraph 129, Pierson).

However Pierson and Butler et al. do not explicitly teach specific use of a packet error counter for counting a number of packets with at least one byte in error detected.

Yu in an analogous art teaches packet error counter (page 13, paragraph 194, Yu) and the IOSL device that contains an 8-bit FIFO counter that counts every packet affected by a FIFO error event (page 13, paragraph 192, Yu).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Yu by including an additional step of using a packet error counter for counting a number of packets with at least one byte in error detected.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a packet error counter for counting a number of packets with at least one byte in error detected would provide the opportunity to detect data transmission errors.

- As per claim 50, Pierson, Butler et al. and Yu teach the additional limitations.

Yu teaches counting a number of packets with a byte in error detected (page 13, paragraph 192, 194, Yu).

Pierson also teaches the bit error rate testing (page 11, paragraph 129, Pierson).

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8. Claims 9-12, 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson (US 2003/0048781 A1) and Butler et al. (US 6,438,717 B1) as applied to claim 1 above, and further in view of Mejia et al. (US 2003/0009307 A1).

As per claim 9, Pierson and Butler et al. substantially teach the claimed invention described in claim 1 (as rejected above). Pierson also teaches the integrated packet bit error rate tester (page 11, paragraph 129, Pierson). Butler et al. teach the second memory that captures the received packet data (fig. 1, col. 2, line 53 to col. 3, line 16, Butler et al.).

However Pierson and Butler et al. do not explicitly teach specific use of detecting a pre-programmed pattern.

Mejia et al. in an analogous art teach a programmable signal generating mechanism (page 2, paragraph 25, Mejia et al.) and most test instruments expect the same test pattern back that it sent (page 3, paragraph 41, Mejia et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pierson's patent with the teachings of Mejia et al. by including an additional step of detecting a pre-programmed pattern.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting a pre-programmed pattern would provide the opportunity to compare the received pattern with the transmitted pattern to determine data transmission errors.

- As per claim 10, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Mejia et al. teach that the pre-programmed pattern includes a fixed pattern (page 3, paragraph 41, Mejia et al.).

- As per claim 11, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Mejia et al. teach that the pre-programmed pattern includes a programmable pattern (page 2, paragraph 25, Mejia et al.).

- As per claim 12, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

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Butler et al. teach that the pre-programmed pattern includes a CRC pattern (col. 3, lines 3-7, lines 29-30, Butler et al.).

- As per claim 31, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Pierson teaches the integrated packet bit error rate tester (page 11, paragraph 129, Pierson). Butler et al. teach the second memory that captures the received packet data (fig. 1, col. 2, line 53 to col. 3, line 16, Butler, et al.). Mejia et al. teach detecting a pre-programmed pattern (page 2, paragraph 25, page 3, paragraph 41, Mejia et al.).

- As per claim 32, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Mejia et al. teach that the pre-programmed pattern includes a fixed pattern (page 3, paragraph 41, Mejia et al.).

- As per claim 33, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Mejia et al. teach that the pre-programmed pattern includes a programmable pattern (page 2, paragraph 25, Mejia et al.).

- As per claim 34, Pierson, Butler et al. and Mejia et al. teach the additional limitations.

Butler et al. teach that the pre-programmed pattern includes a CRC pattern (col. 3, lines 3-7, lines 29-30, Butler et al.).

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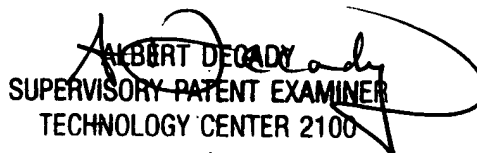
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Patent Examiner



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